

Lab no 06: XOR gate and Half adder using a NAND IC

The purpose of this Lab is to:

- Design an XOR gate and simulate it on Proteus simulator.
- Use NAND IC to implement an XOR gate on the breadboard.
- Design and Implement Half adder.

Required Components

- Breadboard.
- 5V battery.
- Jumper wires.
- 330-ohm Resistor.
- LEDs.
- 2 NAND IC 7400.

Parts:

- 1. Logic Gate Simulation.
- 2. Design and Implement an XOR gate using NAND IC.
- 3. Design and Implement Half adder.



Part 1: Logic Gate Simulation

In this Part, you will learn to use proteus for circuit simulation.

- Download Proteus software (<u>Here</u>).
- Install Proteus software. (<u>Steps</u>)
- Open a new project

click file -> new project or



- Add device and select the following items
 - 1. Logic-toggle (switch)
 - 2. 7400 (NAND IC)
 - 3. Logic-probe (output)

Project - Proteus 8 Professional - Schematic Capture				
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Keywor <u>d</u> s:	Besults (251):			74S80 Preview:
nand	Device	Library	Description	 Schematic Model [74NAND2.MDF]
Match Whole Words?	24500	745	Quadruple 2-Input Positive-NAND Gates	
Show only parts with models?	74S00.DM	745	Quadruple 2-Input Positive-NAND Gates	
Catogory	74S00.IEC	74S	Quadruple 2-Input Positive-NAND Gates	
Calegoly.	74503	74S	Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs	
CMOS 4000 series	74S03.IEC	74S	Quadruple 2-Input Positive-NAND Buffer With Open-Collector Outputs	
Modelling Primitives	74S10	74S	Triple 3-Input Positive-NAND Gates	
Optoelectronics	74S10.DM	74S	Triple 3-Input Positive-NAND Gates	
TTI 74 series	74S10.IEC	74S	Triple 3-Input Positive-NAND Gates	
TTL 74ALS series	74S132	74S	Quad 2-Input Schmitt-Triggered NAND Gates 2	2
TTL 74AS series	74S132.DM	74S	Quad 2-Input Schmitt-Triggered NAND Gates	
TTL 74F series	74S132.IEC	74S	Quad 2-Input Schmitt-Triggered NAND Gates	
TTL 74HCT series	74S133	74S	13-Input Positive-NAND Gates	
TTL 74LS series	74S133.DM	74S	13-Input Positive-NAND Gates	
TTL 74S series	74S133.IEC	74S	13-Input Positive-NAND Gates	
	74S134	74S	12-Input Positive NAND Gate With Tristate Output	
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	74S134.IEC	74S	12-Input Positive NAND Gate With Tristate Output	PCB Preview
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	74S140.IEC	74S	Dual 4-input positive-NAND 50-Ohm line drivers	
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	74538	74S	Quad 2-input positive-NAND buffers with open collector outputs	2
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monoconer.	74540	74S	Dual 4-Input NAND Gate With Buffered Output	
	74S40.DM	74S	Dual 4-Input NAND Gate With Buffered Output	
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Build the XOR gate using NAND gates, as shown in Figure.1. Where
 A and B are inputs and Q is the output.



Figure 1: XOR using NAND

- Connect inputs (A and B) to the logic-toggle, as shown in Figure 2.
- Connect the output (Q) to the logic-prob, as shown in Figure 2.
- Run and Simulate the XOR-gate Circuit.
- Verify the XOR-gate output(Q) by toggling the inputs (A and B).



Figure 2:XOR using NAND gates on Proteus Simulator.



Part 2: Design and Implement an XOR gate using NAND.

A 7400 is a quad NAND gates chip. This means it contains 4 NAND gates inside it, as shown in Figure 3.



Figure 3. NAND Gate IC, Schematic, Pin Configuration, and truth table.

In Figure 4, Input A is represented by the green wire and Input B is represented by the yellow wire.

<u>Steps:</u>

- As shown in Figure 3, 7400 Pin 7 is the ground and Pin 14 is VCC. So, <u>Connect</u> 7400 Pin 7 to the ground line, and Pin 14 to the 5V power line, as shown in Figure 4.
- <u>Connect</u> the Inputs of the first NAND gate, Input A1 (Pin 1) to the Ground (logic 0) the yellow wire (A), and Input B1 (Pin 2) to the 5V power (logic 1) the Green wire(B).
- <u>Connect</u> the Inputs of the second NAND gate, Input A2 (Pin 4) to Output Y1 (Pin 3) and Input B2 (Pin 5) to the Ground (logic 0) the yellow wire (B).
- <u>Connect</u> the Inputs of the third NAND gate, Input A3 (Pin 9) to Output Y2 (Pin 6), the purple wire. <u>Connect</u> Input B3 (Pin 10) to Output Y4 (Pin 11).
- 5) Connect the Inputs of the fourth NAND gate, Input A4 (Pin 12) to Output Y1 (Pin 3), the orange wire. <u>Connect</u> Input B4 (Pin 13) to the 5V power (logic 1), the green wire (A).

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- 6) Output Y3 (Pin 8) represent Q (output XOR), <u>Connect</u> the output to a LED, as shown in Figure 4.
- 7) Verify the output of the Circuit. When LED is ON/OFF?



Figure 3:NAND IC to design XOR gate in breadboard.

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Part 3: Design and Implement Half adder.

The half-adder accepts two binary digits on its inputs and produces two binary digits on its outputs—a sum bit and a carry bit.

Half-Adder



Simulate Half-adder on Proteus:

- Connect inputs (A and B) to the logic-toggle, as shown in Figure 5.
- Connect the output (SUM and CARRY) to the logic-prob, as shown in Figure 5.
- Run and Simulate the Half Adder.
- Verify the Half Adder outputs (SUM and CARRY) by toggling the inputs (A and B).



Figure 5: Half Adder using NAND by Proteus

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In Figure 6, Input A is represented by the green wire and Input B is represented by the yellow wire.

<u>Steps:</u>

<u>connect first nand ic</u>

- 1) As shown in Figure 3, 7400 Pin 7 is the ground and Pin 14 is VCC. So, <u>**Connect**</u> 7400 Pin 7 to the ground line, and Pin 14 to the 5V power line, as shown in Figure 6.
- <u>Connect</u> the Inputs of the first NAND gate, Input A1 (Pin 1) to the Ground (logic 0) the yellow wire (A), and Input B1 (Pin 2) to the 5V power (logic 1) the Green wire(B).
- 3) <u>Connect</u> the Inputs of the second NAND gate, Input A2 (Pin 4) to Output Y1 (Pin 3) and Input B2 (Pin 5) to the Ground (logic 0) the yellow wire (B).
- <u>Connect</u> the Inputs of the third NAND gate, Input A3 (Pin 9) to Output Y2 (Pin 6), the purple wire. <u>Connect</u> Input B3 (Pin 10) to Output Y4 (Pin 11).
- Connect the Inputs of the fourth NAND gate, Input A4 (Pin 12) to Output Y1 (Pin 3), the orange wire. <u>Connect</u> Input B4 (Pin 13) to the 5V power (logic 1), the green wire (A).
- 6) Output Y3 (Pin 8) represent SUM, <u>**Connect**</u> the output to a blue LED, as shown in Figure 6.
- <u>connect second nand ic</u>
 - 1) <u>Connect</u> the Inputs of the first NAND gate, Input A1 (Pin 1) to Output Y1 (Pin 3) in the first ic and Input B1 (Pin 2) to Output Y1 (Pin 3) in the first ic
 - 2) Output Y1 (Pin 3) represent CARRY, <u>Connect</u> the output to a red LED, as shown in Figure 6.

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Figure 6:NAND IC to design Half Adder on breadboard.

<u>Note</u>

- ✤ Lab XOR gate using a NAND IC video (<u>Here</u>)
- ✤ Install Proteus software (<u>Here</u>)
- Example on Proteus (<u>Here</u>)
- ICS datasheets, Simulator, Proteus download (<u>Here</u>)
- XOR using NAND Gate XOR using NAND Gate | Tinkercad
- Half Adder using NAND half adder using NAND Gate | Tinkercad